IN THE CLAIMS:

A listing of the claims follows. The claims are in the format required by 35 C.F.R. §1.121.

1. (Original) A system comprising:

a plurality of digital audio controller chips; and

a synchronization line connected to each of the plurality of chips;

wherein one of the plurality of chips is a master, and the remainder of the plurality of chips are slaves

wherein the master is configured to generate a synchronization signal on the synchronization line

wherein each of the slaves is configured to detect the synchronization signal and to begin synchronized operation in response to detecting the synchronization signal.

2. (Original) The system of claim 1, wherein the plurality of digital audio controller chips comprise pulse width modulation (PWM) controller chips in a multi-chip audio amplification system.

3. (Original) The system of claim 1, wherein the master is configured to detect the synchronization signal and to begin synchronized operation in response to detecting the synchronization signal.

4. (Original) The system of claim 1, wherein the master is designated during an initialization process.

5. (Original) The system of claim 1, wherein the master and the slaves have identical circuitry.

6. (Original) The system of claim 1, wherein the synchronization signal comprises a transition from a passive state to an active state.

7. (Original) The system of claim 6, wherein the master is configured to repeat the transition at a fixed intervals.

8. (Original) The system of claim 7, wherein the master is configured to maintain the active state for a fixed period after each transition.

9. (Original) The system of claim 8, wherein each slave is configured to sample the synchronization line during the fixed period to determine whether the synchronization line is in an active state.

10. (Original) The system of claim 9, wherein each slave is configured to take multiple samples during the fixed period and to determine whether the synchronization line is in an active state based upon a majority of the multiple samples.

11. (Original) The system of claim 9, wherein each slave is configured to detect the transition from the passive state to the active state by sampling the synchronization line at a first rate and to sample the synchronization line during the fixed period at a second rate which is less than the first rate.

12. (Original) The system of claim 9, wherein each slave is configured to filter samples of the synchronization line.

13. (Previously presented) The system of claim 1, wherein the master is configured to transmit non-synchronization data to the slaves via the synchronization line.

14. (Original) The system of claim 13, wherein the synchronization signal comprises a transition from a passive state to an active state, wherein the master is configured to maintain the active state for a fixed period, then transition from the active state to the passive state, then maintain the passive state for a fixed period, then transmit data.

15. (Original) The system of claim 1, wherein each of the slaves is configured to determine whether an error has occurred and, in response to detecting an error, to cause the master to re-synchronize the slaves.

16. (Original) The system of claim 15, wherein causing the master to re-synchronize comprises driving the synchronization line to the active state.

17. (Original) The system of claim 1, wherein the system is configured to align a phase of an output of each controller chips by synchronizing the slaves with the master and to then stagger each of the phases.

18. (Original) The system of claim 1, wherein the master is configured to determine whether all of the slaves are ready to begin synchronized operation before generating the synchronization signal.

19. (Original) The system of claim 18, wherein each of the slaves is configured to drive the synchronization line to an active state until the slave is ready to begin synchronized operation, and wherein the master is configured to determine that all of the slaves are ready to begin synchronized operation if the synchronization line is in a passive state.